Design and harware implementation of Memory-Polynomial Model based on DSP board

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Abstract. This paper presents a Memory-Polynomial Model as Special case of Volterra Series implemented in Hardware using a DSP board. The implementation uses Matlab/Simulink, and the DSP Development Kit Cyclone III Edition. The first stage is to develop the model in Matlab/Simulink Environment using the DSP Builder Blockset through the Signal compiler block, after that the design is downloaded to the DSP Board. The results show that this simulation technique is able to prove the effectiveness of the MPM as behavioral model for Power Amplifiers.

1 Introduction

The Power amplifier (PA) is the most important component in a Radio Frequency link, unfortunately it is inherently nonlinear generating spectral regrowth when its behavioral modeling is not properly developed, and the memory and intermodulation effects are not considered during the modeling. The Memory Polynomial Model (MPM) as special case of the Volterra Series is an adequate method to model the PA behavior. The Volterra are power series with memory [1], by its internal architecture tends to increase the required parameters to develop a behavioral modeling for Power Amplifiers, this condition leads to use a special case as MPM improving the computational processing time during the modeling, and they consider undesirable effects as memory and non-linearity before the circuit fabrication. Some works have been presented with reformulated Volterra Series as [2] reducing the processing time. The main idea of this work is not to prove the computational time cost reduction as [3] reducing the required parameter for an accurate model identification based on the MPM proving that this truncation of the Volterra Series is able to reduce the internal iterations during the modelling. This work is focused in the implementation stage in Hardware using s DSP board. A proper modeling technique for PAs is very profitable because once that the micro-device was manufactured their internal modifications are not allowed, the MPM as modulation technique for PAs assure to introduce these two main undesirable effects prior to the fabrication.

Another important factor is to prove the performance in hardware of this type of modeling, the Field Programmable Gate Array (FPGA) has flexible structure to process signals and processes related to MPM.

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The FPGA has many advantages in digital signal processing and flexible implementation, the DSP (Digital Signal Processing) Builder Blockset in Simulink is able to convert a system architecture to VHSIC hardware description language (VHDL) code for the compilation and synthesis in Altera environment. Some works related to implementation in FPGA have been developed during recent years [4], [5], [6].

The structure of this article is organized as follows: Section 2 presents the general Volterra series and the implemented MPM into the DSP Design. The Section 3 shows the design procedure of the Memory-Polynomial Model. This section includes the implemented model into Simulink environment based in Altera DSP Builder blocks. In the Section 4 hardware implementation was done. The conclusions are drawn in Section 5.

2 Behavioral Modeling: Volterra Series

A characteristic of the Volterra Series as behavioral modeling is that if the input signal bandwidth becomes wider, and the memory effects of the power amplifier are considered, then the computational time increases in relation with the input width. The Volterra Series is a precise behavioral model to describe nonlinear HPAs [7], and can be expressed as:

$$y(n) = \sum_{k} \sum_{l_1} \cdots \sum_{l_{2k+1}} h_{2k+1}(l_1, l_2, \ldots, l_{2k+1}) \prod_{i=1}^{k+1} x(n-\tau_i) \prod_{i=k+2}^{2k+1} x^*(n-\tau_i) d\tau_{2k+1} \quad (1)$$

where

$x(n)$ is the input complex base-band signal.

$x^*(n)$ is the complex conjugate of the input complex base-band signal.

h_k are complex valued parameters.

2.1 Memory-Polinomial Model

The MPM as special case of the Volterra Series is able to consider the undesirable memory effects and non-linearities that affect the spectral regrowth during the behavioral modeling, the MPM structure is showed in equation (2):

$$y(n) = \sum_{q=0}^{Q} \sum_{k=1}^{K} a_{2k-1,q} |x(n-q)|^{2(k-1)} x(n-q) \quad (2)$$

where

$x(n)$ is the input complex base-band signal.

$y(n)$ is the output complex base-band signal.

$a_{k,q}$ are complex valued parameters.

Q is the memory depth.

K is the order of the polynomial.

Based on the equation (2) each stage of the MPM can be represented in Figure (1).

Each stage of the MPM can be subdivided depending of the sampling made for the input signal. Figure (2) shows the internal structure and the delay made for each

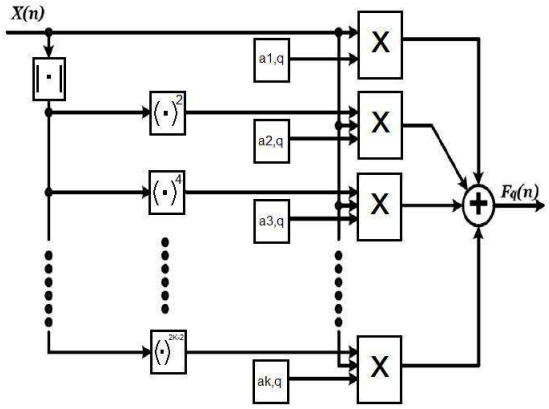

Fig. 1. MPM Internal Blocks during each stage

step. This body creates a phase offset of the signal inevitable during the first cycle and represent the general overview of this model type.

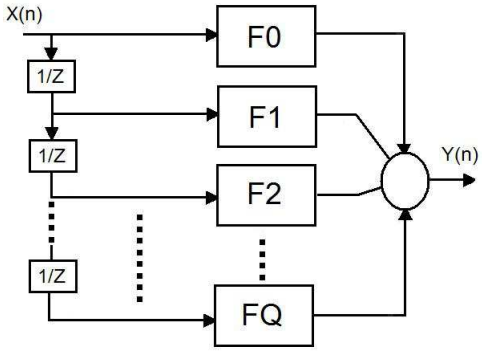

Fig. 2. MPM Subdivided for each sample of the input signal

3 Memory-Polynomial Model Implementation

The DSP Development Kit Cyclone III Edition delivers a complete digital signal processing (DSP) development environment; it includes the Cyclone III development board and Quartus II development software. The system operates with an internal clock of 50 MHz provided by a PLL (Phase-Locked Loop) circuitry. There are some works related to DSP Builder implementation [8], [9] and others applied to control systems [10].

The MPM explained in the previous section was created for a sine wave signal but can be implemented for digital or analog modulated signals as AM, FM or QAM

signals, some works have demonstrated that the MPM is able to work even for RF applications [11]. Figure (3) shows a general overview of the developed system in Simulink including the Signal Compiler icon and the Signal Tap Logic Analyzer making and interface with Quartus II Software for the synthesis, fitter and program process.

In this design, a generated sine wave is included by an internal LUT (Look up Table) and it is related with the capability of 14 bits of the DAC located in the HSMC card the signal is able to reach a value from 0 to 16384 due to the DAC sampling. This sine wave is attenuated and amplified 30 dB by the created MPM with the purpose of showing the effectiveness of the MPM using the DSP Builder Blockset, Figure (4) shows an overview of the developed MPM. Figure (5) shows the amplified signal by the MPM, as it can see there is a phase offset caused by the internal structure of the MPM, but the whole information is recovered after the second cycle.

Figure (4) shows the Hardware compilation steps made in Quartus II Software and Figure (6) the Simulation Waveform of LUT being monitored by Signal Tap Logic Analyzer included for the DSP Board.

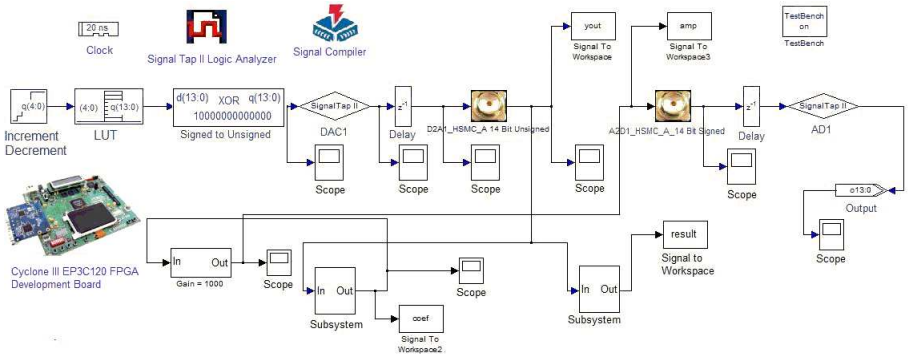

Fig. 3. Schematic Overview

The DSP Builder Signal Compiler block reads Simulink Model Files (.mdl) that are built using DSP Builder blocks and generates VHDL files and Tcl scripts for synthesis, hardware implementation, and simulation [12].

Once that the system was completed in Simulink the Signal Compiler Blockset allows to make the analyze, synthesis, fitter and programming process as a interface between Simulink and Quartus II Software, the section Export in this blockset has the property to export the valid HDL code. The VHDL or HDL code is a hardware description language used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits.

4 Results

The generated sine wave by an internal LUT was implemented in the developed MPM and the signal was amplified 1000 times, the generated signal by the 14 bits DAC was

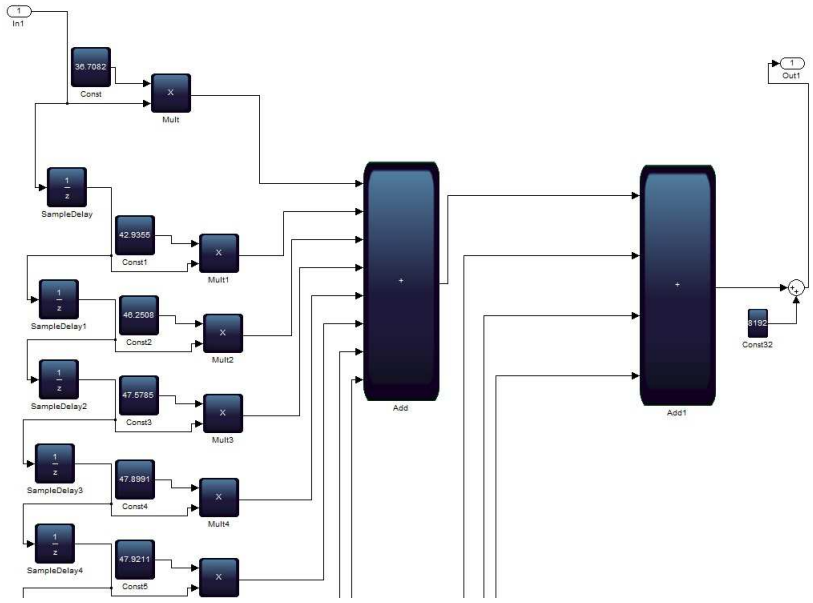

Fig. 4. Memory-Polynomial Model using the DSP Builder Blockset

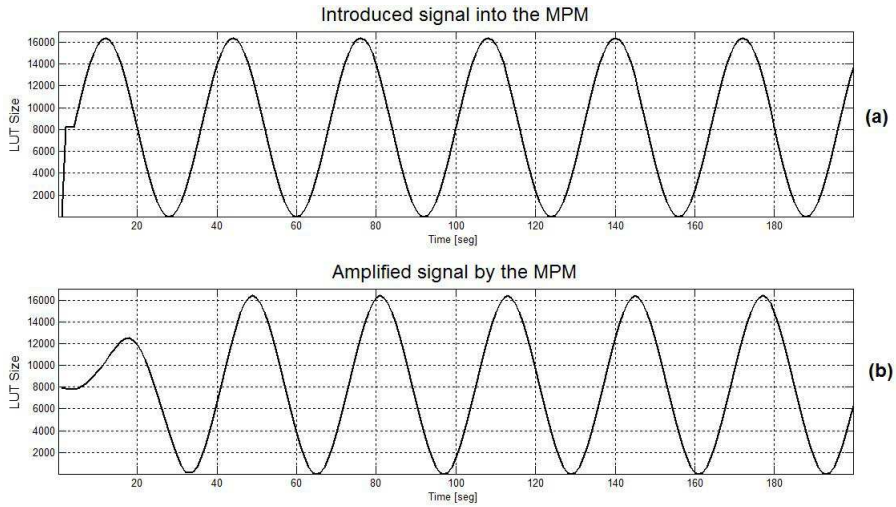

Fig. 5. (a) Generated signal by the LUT and (b) Recovered signal by the MPM

recovered by the amplification and the information passed though the communication between the DAC and ADC in the HSMC board.

The internal 50 Mhz clock was used in this work. The implemented MPM over the DSP Builder was properly developed using the DSP Builder Blockset.

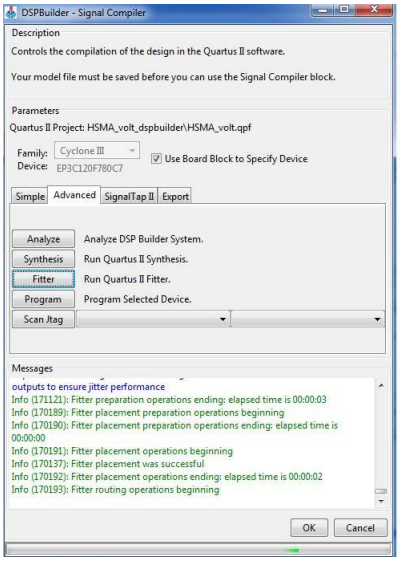

Fig. 6. Hardware compilation steps

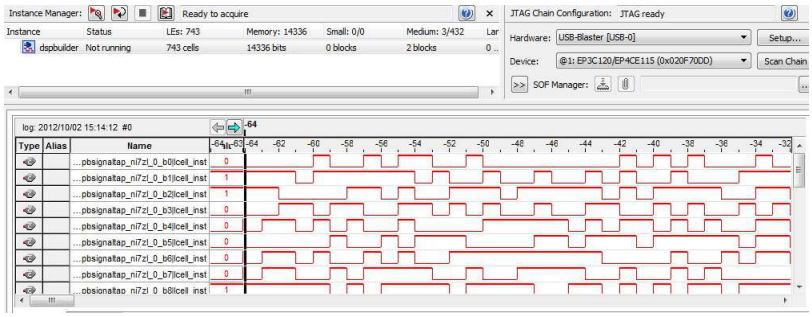

Fig. 7. Simulation waveform of LUT

5 Conclusion

In this paper, the Memory Polynomial Model as special case of the Volterra Series is implemented in the DSP Development Kit, Cyclone III Edition, the reduction of computational complexity together with the fast processing involved in the FPGA Cyclone III gives a proper behavioral modeling for HPAs and leaves open the option to introduce digitally/analogically modulated signals making wider the necessary process to modeling them.

The General Volterra Series is a precise method to create a behavioral modeling but how it was explained in this work the number of coefficients of the Volterra series increases exponentially as the memory length and the nonlinear order increase driving us to consider a Special case of the Volterra Series as the MPM, even better to create

an structure based on an FPGA as Altera Cyclone III to prove the performance of the MPM in Hardware implementation.

This stage was made using the DSP Builder technology allow us go from the system scheme to the VHDL files for synthesis and hardware implementation in the Cyclone III FPGA,. The MPM amplified the signal 30 dB using the internal clock with frequency of 50 MHz.

The computational time reduction and the eliminated internal iterations were not proved in this work, but as was referenced in the introduction section the MPM is able to achieve an accurate model of the PA reducing the processing time.

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